Electric field induced metallic behavior in thin crystals of ferroelectric *α*-In2Se3

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Abstract

Ferroelectric semiconductor field effect transistors (FeSmFETs), which employ ferroelectric semiconducting thin crystals of *α*-In2Se3 as the channel material as opposed to the gate dielectric in conventional ferroelectric FETs (FeFETs) were prepared and measured from room to the liquid-helium temperatures. These FeSmFETs were found to yield evidence for the reorientation of the electrical polarization and an electric field induced metallic state in *α*-In2Se3. Our findings suggest that FeSmFETs can serve as a platform for the fundamental study of ferroelectric metals as well as the exploration of potential applications of semiconducting ferroelectrics.

Ferroelectricity is defined by the formation of spontaneous electrical polarization in a non‑centrosymmetric crystal and the reorientation of the polarization between crystallographically defined directions by the application of an external electric field[[1]](#endnote-2). Ferroelectrics have been used to store data in either a capacitor or a ferroelectric field-effect transistor (FeFET)[[2]](#endnote-3),[[3]](#endnote-4) configuration, the latter of which features a ferroelectric gate dielectric and a non-ferroelectric semiconducting channel. FeFETs provide not only fast and non-volatile data storage, but also a pathway towards “logic in memory” functions. However, the commercialization of FeFETs has encountered multiple obstacles ranging from retention time originating from the depolarization field and the gate leakage current[[4]](#endnote-5) to endurance limited mainly by interface charge traps[[5]](#endnote-6). A FeFET variation which replaces the semiconducting channel in the conventional FET with a *ferroelectric* semiconducting channel but retains the non-ferroelectric gate dielectric was demonstrated recently[[6]](#endnote-7). This produces an “on” (or “off”) state without an applied gate voltage, similar to a traditional FeFET. Such a device is referred to as a ferroelectric semiconductor field effect transistor (FeSmFET).

It is interesting to ask whether the “on” state in the FeSmFET can be a metallic state, which will make the transition from the “on” to the “off” state a ferroelectric metal-insulator transition. Anderson and Blount[[7]](#endnote-8) examined the structural transition found in metallic V3Si and suggested that the formation of ionic displacements along a polar axis, which led to the loss of inversion symmetry, would be required for the occurrence of the apparent continuous phase transition seen in V3Si. Furthermore, they suggested that such a state should be called a “ferroelectric metal.” Being a metal appears to be inconsistent with the accepted definition of ferroelectricity as mobile charge carriers in a bulk metal will effectively screen any electric field, making the reorientation of the polarization unlikely. Nevertheless, metals showing the presence of electrical dipoles from ionic displacements along with a well-defined polar axis, such as LiOsO3[[8]](#endnote-9),[[9]](#endnote-10), Ca3Ru2O7[[10]](#endnote-11), and other materials[[11]](#endnote-12), have attracted much attention in recent years even though the issue of whether the dipoles found in these materials are spontaneously ordered and reversable has not been resolved. Interestingly, the difficulty in reversing the polarization in a metal can be circumvented for a ferroelectric 2D crystal. A vertical electrical field, applied to a 2D crystal of 1T’-WTe2 by a top and a bottom gate, was shown to lead to sharp jumps in sample conductance, which was attributed to polarization reversal[[12]](#endnote-13). However, direct evidence for ferroelectricity in 2D 1T’-WTe2 is still lacking.

In2Se3, a layered transition metal chalcogenide (TMC) featuring a van der Waals interlayer coupling and an energy gap of 1.4 eV, was predicted[[13]](#endnote-14) to be ferroelectric down to 1-unit-cell thickness in both *α*- and *β*-phases. Supporting evidence for ferroelectricity in In2Se3 was found via piezoelectric force microscopy (PFM)[[14]](#endnote-15),[[15]](#endnote-16),[[16]](#endnote-17),[[17]](#endnote-18),[[18]](#endnote-19) and second harmonic generation (SHG)18,[[19]](#endnote-20),[[20]](#endnote-21), with a transition temperature up to 700 K19. Extensive device work carried out in the last few years also supports ferroelectricity in this layered TMC. An on/off state was found in rectifying devices by sweeping the source-drain voltage14,15,16,17,[[21]](#endnote-22), revealing distinct hysteresis loops suggesting complex orientations of the polarization13,14,16,19. In the pioneering work of the FeSmFET featuring thin crystals of *α*-In2Se3 and a gate dielectric of 90-nm-thick SiO2 or 15-nm-thick HfO2, respectively, large clockwise and counter-clockwise hysteresis loops were found in gate voltage sweeps6. The hysteresis was shown to persist down to 80 mK, making it unlikely that the observed hysteresis at such a low temperature is due to charge traps. These observations strongly support the existence of ferroelectricity in *α*-In2Se3. However, the most explicit demonstration of ferroelectricity in *α*-In2Se3 was obtained in a stacked capacitor/FET device[[22]](#endnote-23). This device consists of monolayer graphene on a SiO2/Si substrate that functions as a bottom gate. The graphene is also the bottom electrode for a capacitor featuring a two-layer dielectric combining an insulating monolayer or bilayer of hexagonal boron nitride (hBN) and an atomically thin, semiconducting crystal of *α*-In2Se3, which was covered by a top metal electrode/gate. The electric field applied between the graphene and the top electrode was used to reorient the polarization in *α*-In2Se3. The graphene sandwiched between SiO2 and hBN functioned as a charge detector through the position of the charge neutral point (CNP) in sample resistance *vs*. the gate voltage curves. From the clear and systematic shift in CNP as the polarization was flipped, a polarization value of 0.92 µC/cm2 was estimated under an external field of 5 x 105 V/cm, which is reasonably close to the theoretically predicted13 value of 0.6 µC/cm2.

The in- and out-of-plane resistivities of *α*-In2Se3 crystals grown by a modified Bridgman method used in this work, obtained from 4-point probe on bulk crystals using electrical contacts made by Ag paint, showed a variable-range hopping (VRH) conduction at low temperatures (below ~40 K, see Fig. 1a) after the unintentionally doped charge carriers are frozen out. Thin crystal of *α*-In2Se3 were obtained by mechanical exfoliation from a bulk crystal and deposited onto a heavily doped silicon chip with 300-nm thick thermally grown surface of SiO2. The thickness of a thin crystal of *α*-In2Se3 was determined by atomic force microscope (AFM) after the transport measurements were carried out. Two types of FeSmFET featuring a Hall bar (Fig. 1e) and traditional FET (Fig. S1a in Supplementary Materials (SM)) pattern, respectively, were prepared by photolithography with electrodes of 5 nm of Ti and 45 nm of Au. The parameters for the four devices used in the present study are shown in Table S1 in SM. DC Electrical transport measurements were carried out in a Quantum Design Physical Property Measurement System (PPMS) equipped with a 9 T superconducting magnet that features a base temperature of 1.8 K. For temperature varying measurements, the device was cooled/warmed at zero gate voltage unless otherwise specified.

To characterize the thin crystals of *α*-In2Se3,Raman spectroscopy, photoluminescence (PL) and second harmonic generation (SHG) measurements were used. The Raman spectra (Fig. 1b) confirmed that the crystals used were *α*-In2Se3[[23]](#endnote-24). An energy gap value of 1.4 eV was revealed in the PL measurements (Fig. 1c), consistent with that found in the literature23. Strong SHG signals with the expected six-fold symmetry were also found (Fig. 1d), demonstrating that our *α*-In2Se3 crystal indeed belongs to the *R3m* space group17,18,19.

Source-drain current *vs*. voltage (*I*D *vs*. *V*DS) characteristics were measured on the FeSmFETs at fixed gate voltages (*V*G). The results for Sample A (Fig. 1e) with a channel length of 12 µm and thickness of 110 nm are shown in Fig. 2 for *V*G increasing from ‑75 to 75 V and back to ‑75V. No saturation in *I*D was observed in this range of the gate voltage up to 10 V for all *V*G values. Given that *I*D for negative *V*G is lower than *I*D for the positive, the *α*-In2Se3 must be *n*-type, consistent with previous observations[[24]](#endnote-25),[[25]](#endnote-26). Similar features in *I*D *vs*. *V*DS characteristics were seen in other samples (Fig. S2). Interestingly, a marked change in the slope was found in most *I*D *vs*. *V*DS curves, showing that *I*D increases much faster at low *V*DS than at high *V*DS values. The sharp rise in *I*D at low *V*DS values (below a few tenth of volts) may be related to the the presence of two back-to-back Schottky diodes studied previously in other materials[[26]](#endnote-27),[[27]](#endnote-28). Behavior seen at high *V*DS values, in particular, in the linear plots (Fig. S2 and S3), is similar to what reported previously6.

Clockwise transfer curves of *I*D *vs*. *V*G, starting at VG = ‑75 V, were measured on our FeSmFET devices at fixed temperatures, *T*, from 300 to 2 K (Fig. 3 and Fig. S5). These results are consistent with those seen in the previous work6. The clockwise hysteresis loop points to the presence of a polarization in the *n*-type *α*-In2Se3 semiconductor. Basically, at a sufficiently large negative *V*G, say, -75 V, the downward pointing electric field will force the polarization inside the *α*-In2Se3 crystal downward (Figs. S1), resulting in *positive* bound surface charge on the *bottom* surface of the crystal due to the presence of the polarization. Consequently, the energy bands will band upward (Fig. S1). The gate voltage induced *positive* charge carriers will deplete the conduction band (the existing negative charge carriers will be “drained” from the channel), which will shut down conduction channels between the source and the drain. On the *top* of the *α*-In2Se3 crystal, however, the *negative* bound charge from the downward pointing polarization will push down the conduction band, placing the Fermi energy within the conduction band (Fig. S1). However, even though the low density of the gate voltage-induced *positive* charge carriers they cannot deplete the conduction band fully because the gate electric field is weak on the top surface of the crystal, no conduction channel between the source and the drain is expected there either because of the low carrier density. An “off” state of the FeSmFET is thus expected, which was indeed observed.

As *V*G increased from the -75 V to 0 and then 75 V, the polarization will start to reverse locally. The depletion layer on the bottom surface of the *α*-In2Se3 crystal will be reduced, helping push down the conduction band. A conduction channel between the source and the drain will eventually be established, leading to the “on” state of the FeSmFET. The device will continue to be in the “on” state as *V*G is increased further to 75 V. Now the polarization will switch to point upward so that the bound charge from the polarization will be negative on the bottom surface of the crystal, featuring negative mobile charge carriers induced by the positive gate voltage. Ramping *V*G from 75 V to 0, the polarization will turn downwards locally, leading to *positive* bound charge from the polarization on the *bottom* surface of the crystal. The existing and gate induced *negative* charge carriers could be bound to the *positive* surface charge from the polarization, creating local areas that are non-conducting. As the gate voltage decreases further, the polarization will continue to flip, leading to continued growth of non-conducting areas and a decreasing *I*D. Eventually all conduction channels disappear, leading to vanishingly small *I*D. A clockwise hysteresis loop as shown in Fig. 3 will be obtained. Our observation is therefore fully consistent with the existence of polarization in *α*-In2Se3, as argued previously6.

The overall hysteresis decreased as the temperature *T* was lowered (Fig. 3). Thus, it is natural to ask whether the reduction in hysteresis was a result of a change in coercive field as the temperature was lowered. This seems to be unlikely given that the ferroelectric transition temperature, Tc, of *α*-In2Se3 was reported to be 700 K19 as the coercive field of a ferroelectric material would increase as *T* is lowered below Tc[[28]](#endnote-29),[[29]](#endnote-30) or stay as a constant far below it. The more likely scenario is the decrease in hysteresis as *T* was lowered was due to the presence of charge traps in our sample. Charge traps in FETs are known to lead to a hysteresis loop. At higher temperatures, the hysteresis originating from charge traps and that from polarization appear to coexist in our samples. However, at a liquid-helium temperature, at which the binding and unbinding of mobile charge carriers from their traps are expected to be suppressed, the observed hysteresis should be only due to the reversal of the polarization, as argued previously6.

Values of two-point resistance *R*DS (= *I*D/*V*DS, taken from the top of the hysteresis loop) are plotted against *T* in Fig. 4a, showing decreasing *R*DS with the lowering *T* and the emergence of a metallic state. The four-point sample resistance, *R*(*T*), of the same crystal was also measured as a function of *T* (inset of Fig. 4a), showing that *R*DS(*T*) and *R*(*T*) have similar behavior. This suggests that the contact resistance between Ti/Au and *α*-In2Se3, which was measured at the room temperature (Fig. S7), did not make a big difference in the behavior of *I*D. Data obtained for *VG* = 75 V in samples B and C showed a positive *dR/dT* at higher temperatures and a complete flattening-off in *R*DS(*T*) down to 4 K (Figs. 4b and S6). A small negative d*R*/d*T* was seen at lowest temperatures in Sample A, even at *V*G = 75 V where the density of gate voltage induced mobile charge carriers is the largest, appears to be due to sample specific disorder. Weak localization in a weakly disordered metallic sample can lead to a negative d*R*/d*T* when *T* is sufficiently low*[[30]](#endnote-31)*. The maximum 2D electric conductivity obtained from the four-point measurements was found to be around 80 *σ*0, where *σ*0 = e2/h (= 4.08 x 10-5Ω-1) is the quantum conductance, e is the electron charge and h is Planck’s constant. Above *σ*0, a negative d*R*/d*T* is expected due to weak localization, along with positive or negative magnetoconductance (MC) depending on the strength of the spin-orbital coupling30. Our measurements showed positive MC at 1.8 K (Fig. 4c), as well as 10 K and 50 K (data not shown), consistent with the weak spin-orbital coupling expected for *α*-In2Se3. The MC data was shown in Fig. 4c to fit Maekawa-Fukuyama theory of 2D weak localization[[31]](#endnote-32) quantitatively.

In the metallic state, the negative mobile charge carriers should be accumulated near the bottom of the *α*-In2Se3 crystal while the rest of the crystal remains semiconducting. This layer of mobile charge will tend to screen the gate electric field, making the polarization in the semiconducting region of the crystal less affected by the gate electric field. However, as shown in the data, some of polarization can still be reoriented by the field even in the metallic state. As a result, the 2D metallic sheet of electrons and the polarization must coexist in *α*-In2Se3.

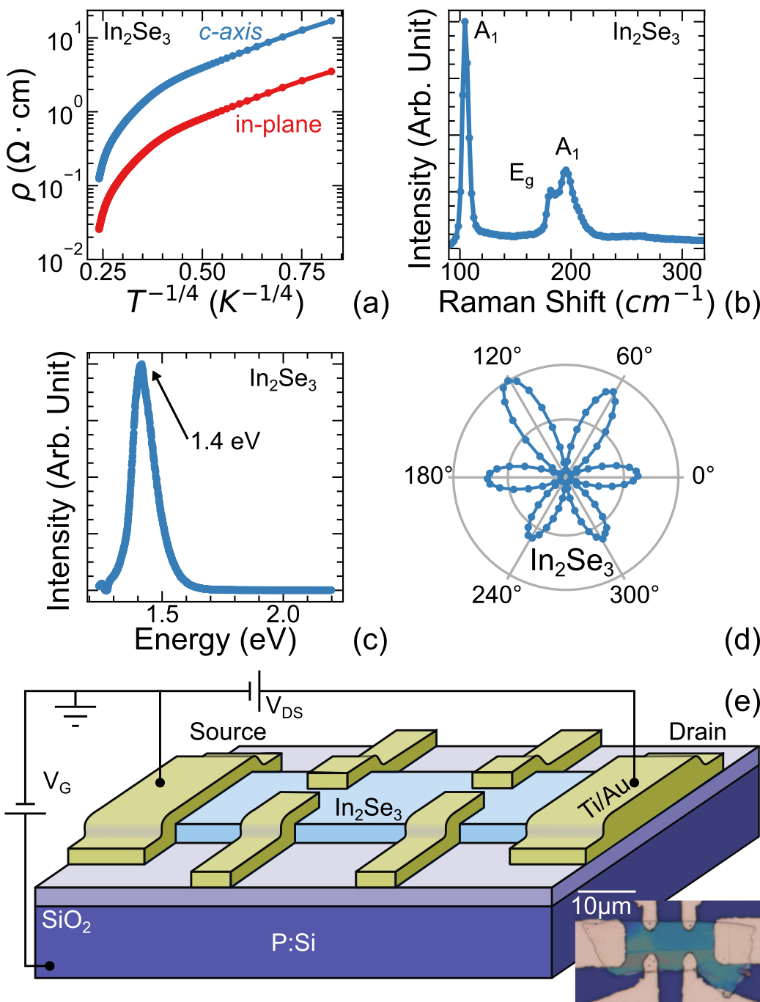
The interesting question is how the bound charge of polarization on the crystal bottom will affect the accumulation of the mobile electrons. At *V*G = 75 V the electric field is expected to induce an electron density of 5 x 1012/cm2. Hall measurements showed that the Hall voltage is a linear function of the magnetic field, suggesting that only electrons are present in the sample. The density of electrons at 4 K is roughly what would be expected solely from that induced by the gate electric field, unaffected by the polarization (Fig. 4d). At higher temperatures however, the electron density obtained by the Hall measurements is larger than that induced by the gate voltage. This is reasonable, as the existing unintentionally doped electrons that are bound to the positive charge traps at low temperatures would start to be released as the temperature was raised, consistent with the observation of the broadening hysteresis noted above.

The observations presented above demonstrate a well-functioning FET with a large *I*D even when gate voltage is at zero. Such a FeSmFET can be used for logic operations as well as a memory device in the microelectronic circuitry with the “logic in memory” functionalities. In addition, ultrathin *α*-In2Se3 was shown to provide a testbed for fundamental research on ferroelectric metals as well as ferroelectric metal-insulator transitions tuned by a gate voltage.

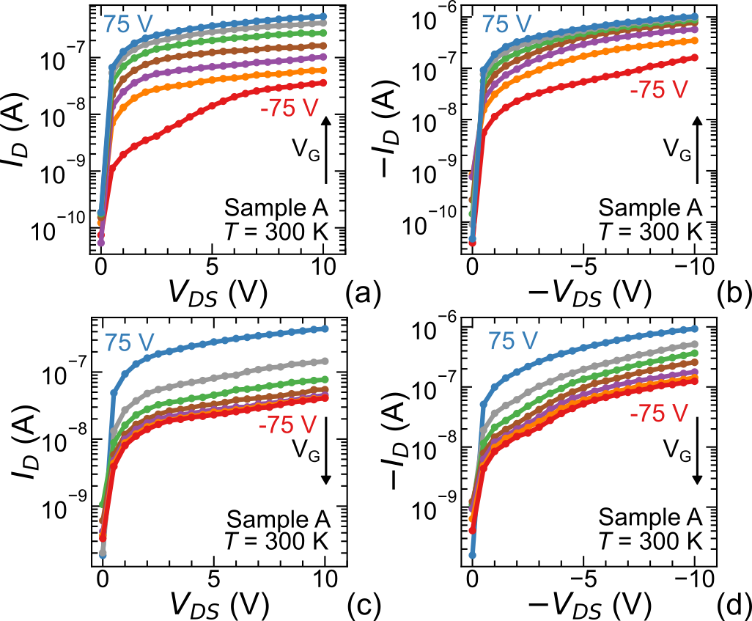
**Acknowledgement**. Work is supported by the NSF (Grant No. EFMA1433378). The *α*-In2Se3 crystals used in this study were produced by the Penn State 2D Crystal Consortium – Materials Innovation Platform (2DCC-MIP) under NSF cooperative agreement DMR-1539916.

**Data Availability.** The data that support the findings of this study are available from the

corresponding author upon reasonable request.



**Fig. 1**. (a) In- and out-of-plane resistivities of bulk single-crystals *α*-In2Se3 showing Mott variable-range hopping conduction behavior, ρin-plane, c-axis (*T*) ~ exp[(T0/*T*)1/4], where T0 is a constant, below around *T* = 160 K. Also shown are results of Raman spectroscopy (b), photoluminescence (c), and second harmonic generation (d) measurements. A schematic of an FeSmFET in the Hall bar pattern is shown in (e). Inset: Optical image of a FeSmFET device following this design with the 10-µm scale bar also shown.

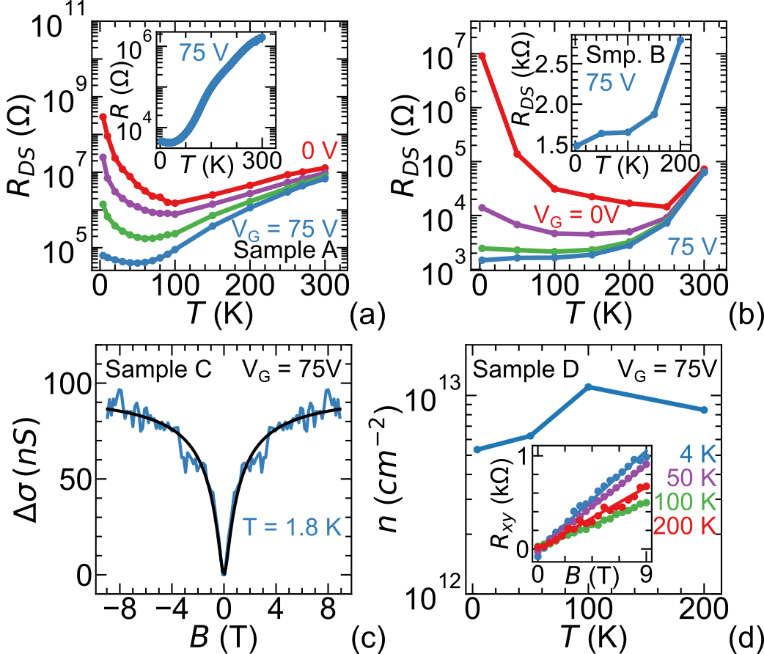


**Fig. 2**. Curves of *I*D-*V*DS for Sample A obtained at room temperature for fixed gate voltages in an increasing order, *V*G = -75, -50, -25, 0, 25, 50, 75 V at a positive (a) and negative (b) values of *V*DS. Corresponding *I*D-*V*DS curves for decreasing *V*G at the same gate voltages are shown in (c) and (d).

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**Fig. 3**. (a-f) Transfer curves of source-drain current *vs*. gate voltage, *I*D *vs*. *V*G, obtained at fixed temperatures (*T*) as indicated. *V*G was initially decreased from 0 to -75 V, after which VG was ramped from –75 to 75 V and then back to –75 V while the *I*D *vs*. *V*G curve was measured. A clockwise hysteresis loop was obtained at each temperature.

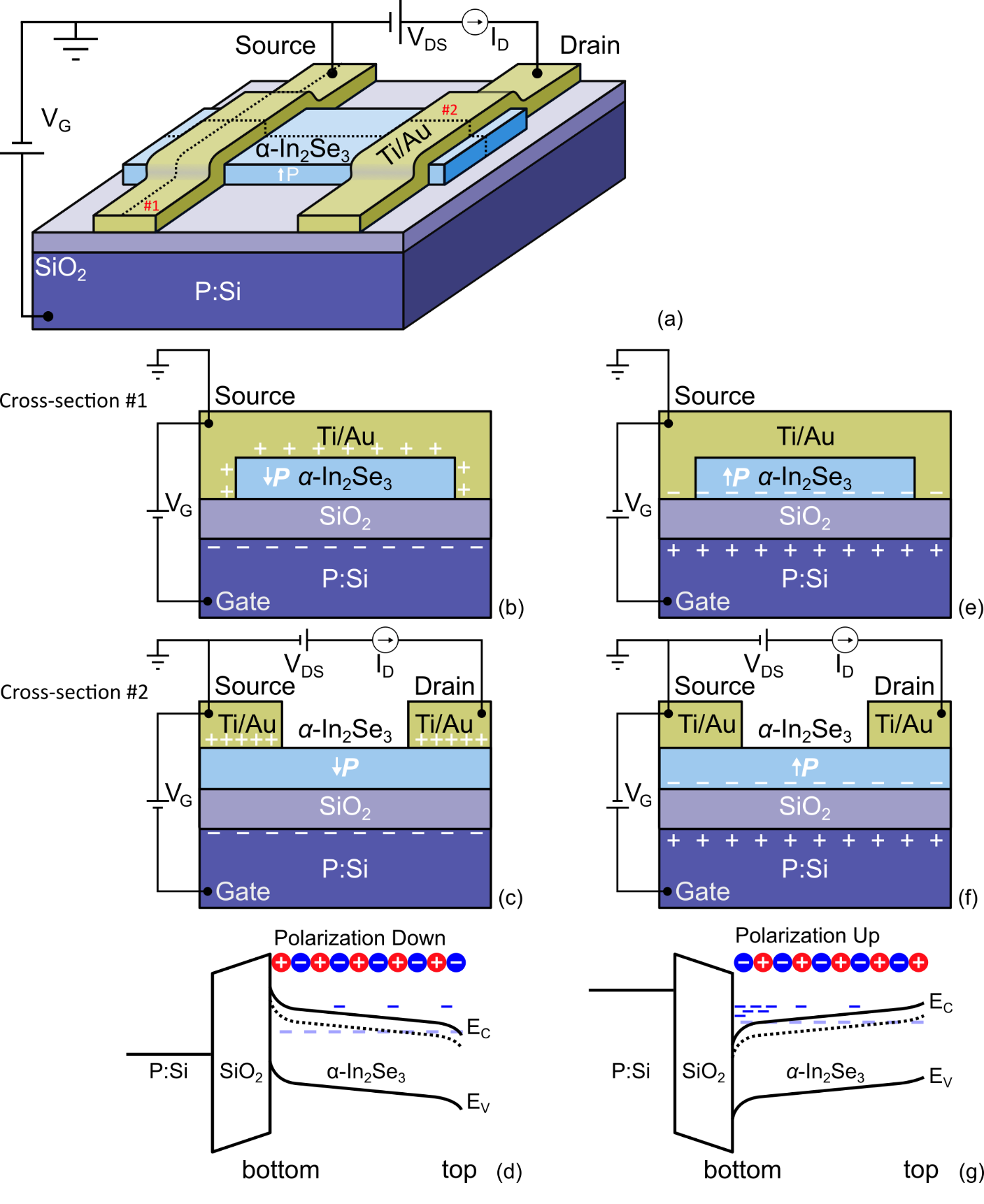


**Fig. 4**. (a) Two-point sample resistance, *R*SD(*T*) (*R*DS = *I*D/*V*DS) obtained at *V*G = 0, 25, 50, and 75 V, in the top portion of the clockwise hysteresis loops taken at fixed temperatures for Sample A. Inset: Four-point resistance *vs*. temperature, *R*(*T*), measured while the device was warming up after it was cooled to 4 K at *V*G = -75 V followed by ramping *V*G from -75 to 75 V at 4 K. (b) *R*DS(*T*) for Sample B in semi-log plot obtained from the top portion of clockwise hysteresis loops. Inset: *R*DS(*T*) for *V*G = 75 V in linear plot. (c) Magnetoconductance at *T* = 1.8 K and *V*G = 75 V for Sample C**.** The Maekawa-Fukuyama theory was shown to fit the data (see main text). (d) Charge carrier density, *n*, as a function of *T* for Sample D. The device design for Samples A and D is shown in Fig. 1e and that for Samples B and C is shown in Fig. S1 (a).

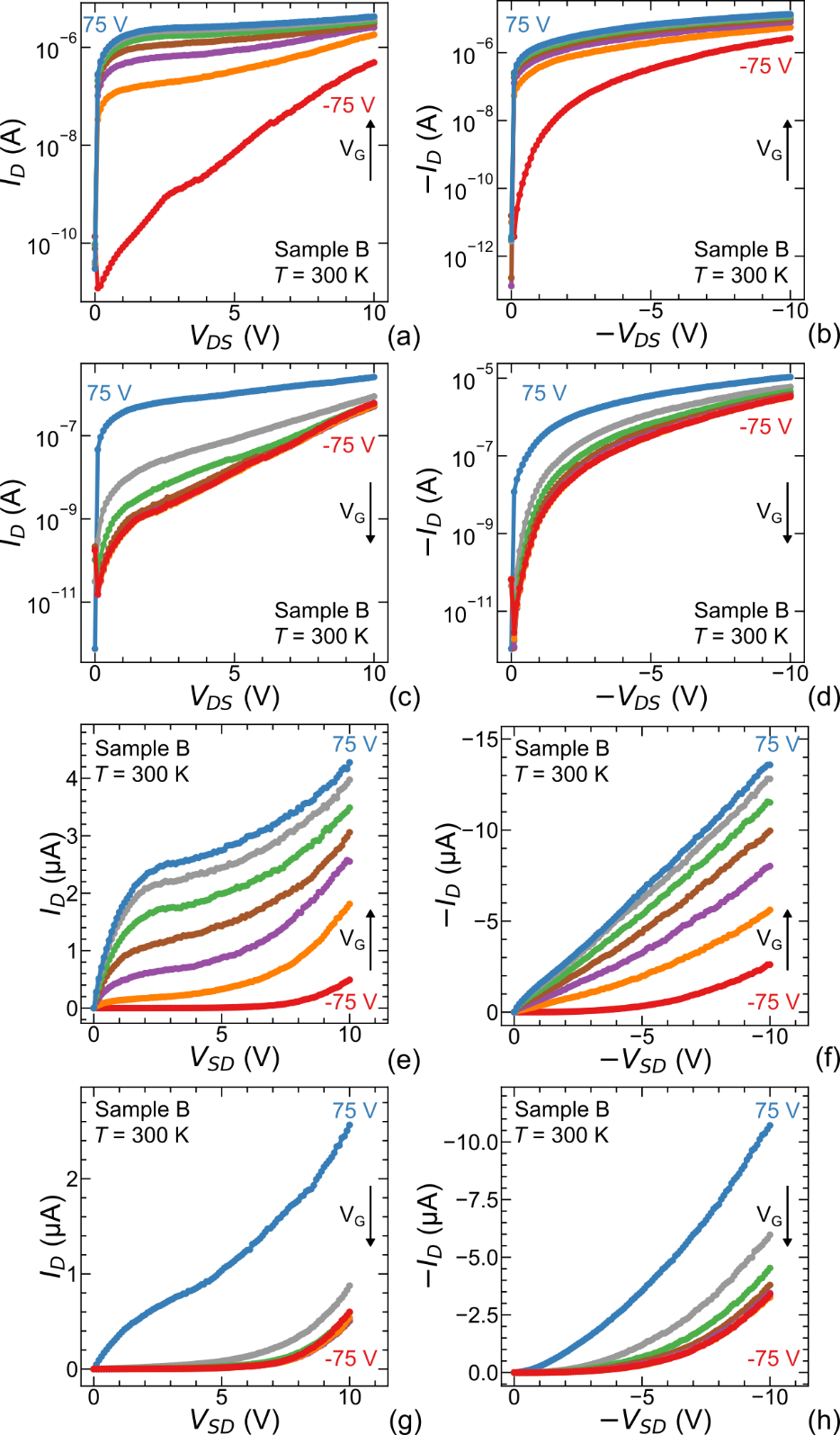
**Supplementary Materials**

**Table S1**. Parameters for 4 devices studied in the current work, where t is the thickness of the *α*-In2Se3 crystal, L is the channel length (length between the voltage leads), w is the channel width, and DVG is the size of the hysteresis loop measured at *I*D = 1 nA and *T* = 300 K.

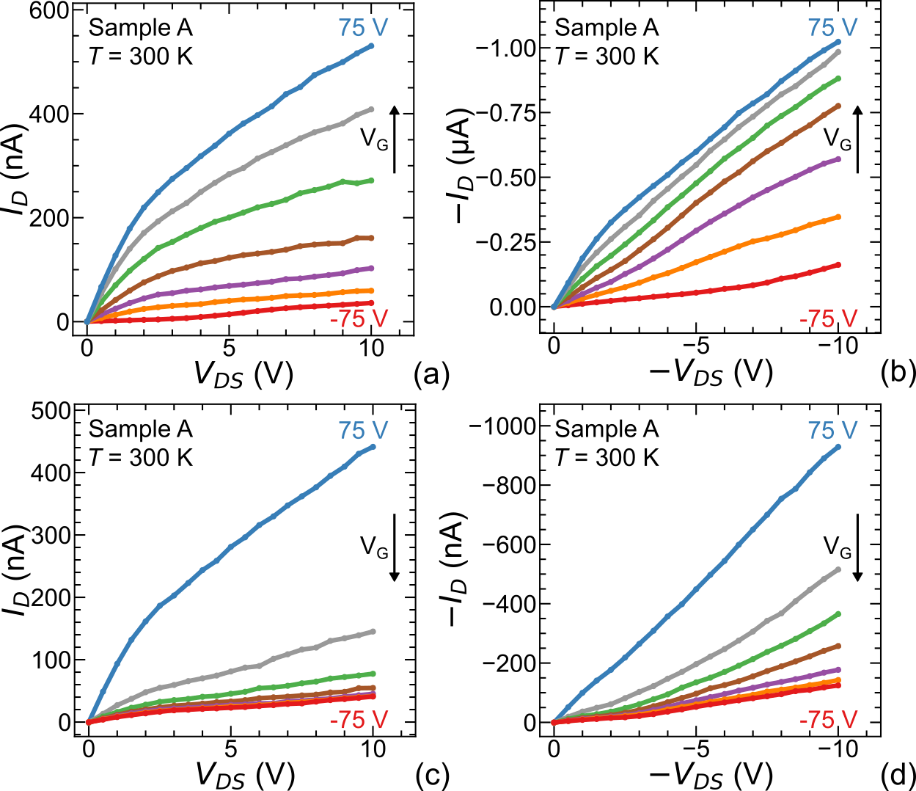
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| --- | --- | --- | --- | --- | --- |
| **Sample** | **t (nm)** | **L (µm)** | **w (µm)** | **Device pattern** | **Δ*V*G (V) at 1nA and 300K** |
| A | 110 | 14 | 10 | Hall bar | 87V |
| B | 13 | 5 | 30 | Standard FET | 19V |
| C | 20 | 2 | 5 | Standard FET | 23V |
| D | 110 | 14 | 9 | Hall bar | not measured |



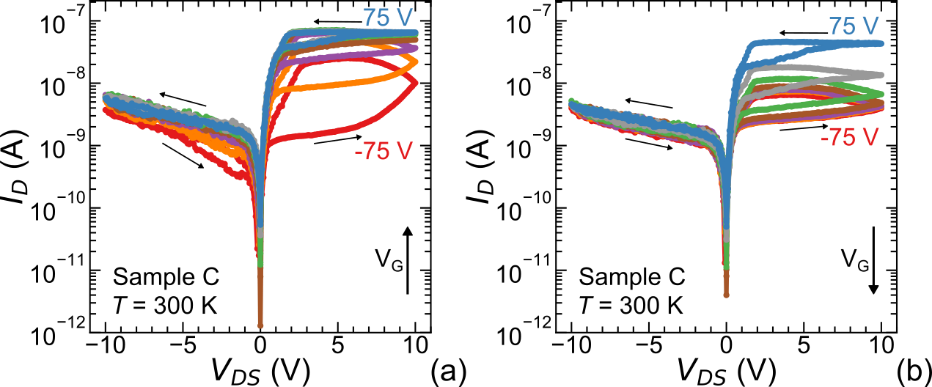
**Fig. S1.** a)Schematic of FeSmFET adopted in Samples B and C. b-c) Cross sectional views of the device cut along the dashed lines marked by #1 and #2 in a), perpendicular to and along the direction of *I*D, respectively, for *V*SD = 0.1 V and *V*SD = -75. The polarization is pointing downwards. d) Band diagrams along the vertical direction in (c) near the center of the *a*-In2Se3 channel is shown for *V*SD = -75 V. The mobile charge carriers are marked by +/- signs while the bound charge from electrical polarization is marked by the +/- circles. The crystal of *α*-In2Se3 is unintentionally doped and *n*-type with the impurity states formed slightly below the bottom of the conduction band (black dashed line). The band bending on the top and bottom surfaces of the *a*-In2Se3 crystal is assumed to be induced by only the bound surface charge from the polarization. The location of the Fermi level (dashed blue line) is determined by the existing charge carriers. The bottom layer of the crystal is depleted at *V*SD = -75 V. e-f) Cross sectional views of the device cut along the dashed lines marked by #1 and #2 in a), respectively for *V*SD = 0.1 V and *V*SD = 75. The polarization is pointing upwards. g) The band along the vertical direction in (f) near the center of the *a*-In2Se3 channel is shown for *V*SD = 75 V. The location of the Fermi level is indicated by blue dashed line. The impurity states are formed slightly below the bottom of the conduction band (black dashed line). The accumulation of mobile electrons near the bottom surface of the crystal, the tilting of the energy band due to the existing of a finite electric field, and the existence of electrons from the impurity states in the interior of the *a*-In2Se3 crystal are shown schematically, when appropriate.



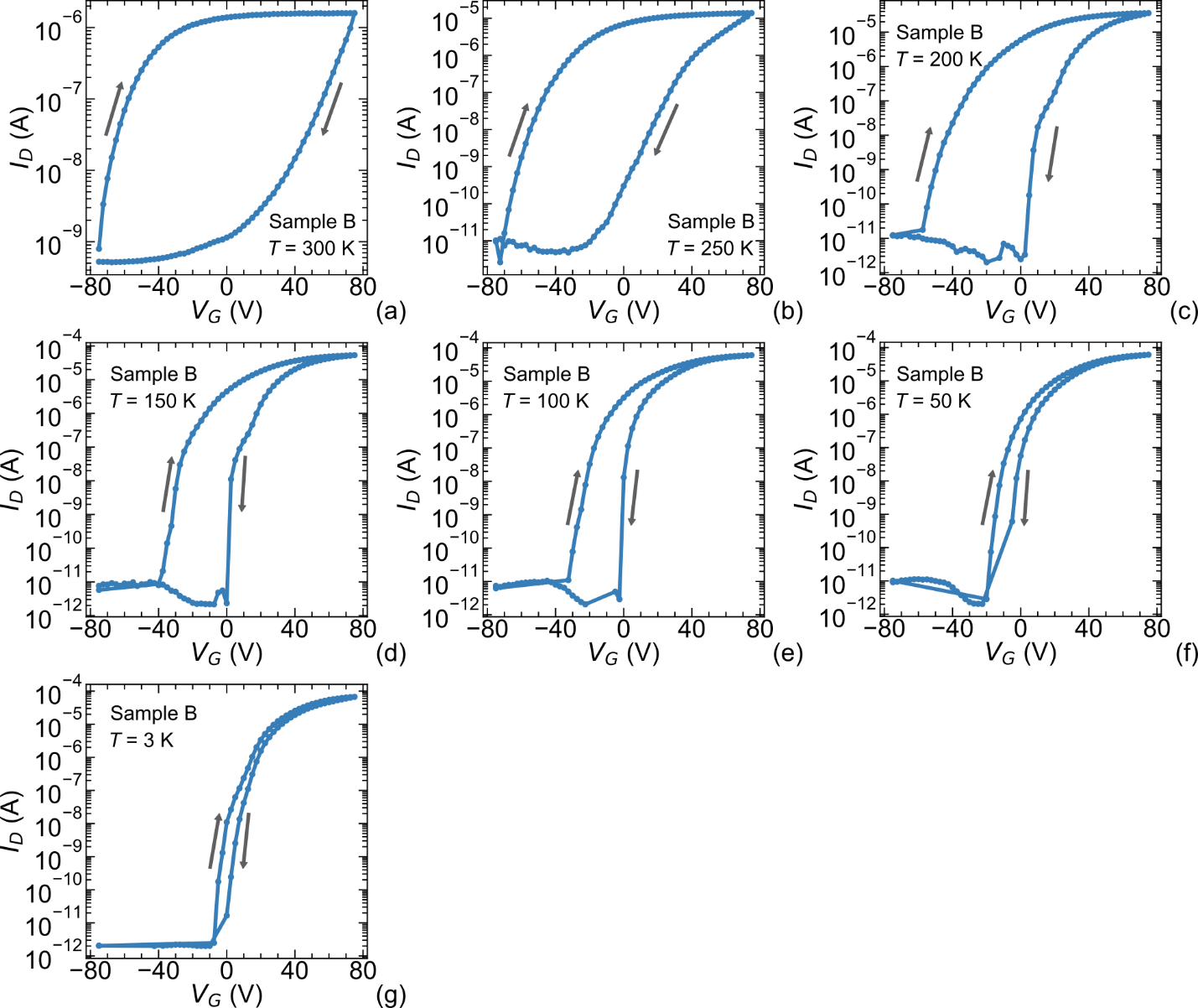
**Fig. S2.** *I*D *vs*. *V*DS measured in Sample B. *VG* was fixed for each curve in 25 V increments from ‑75 V to 75 V, the same as that shown in Fig. 2 in the main text, for positive (a) and negative (b) *VDS*. c-d). Corresponding positive and negative *ID vs. VDS* while *VG* is decreased from 75 V to ‑75 V in 25 V increments. All measurements were done at 300 K. The linear plots of the same data are shown in e-h).



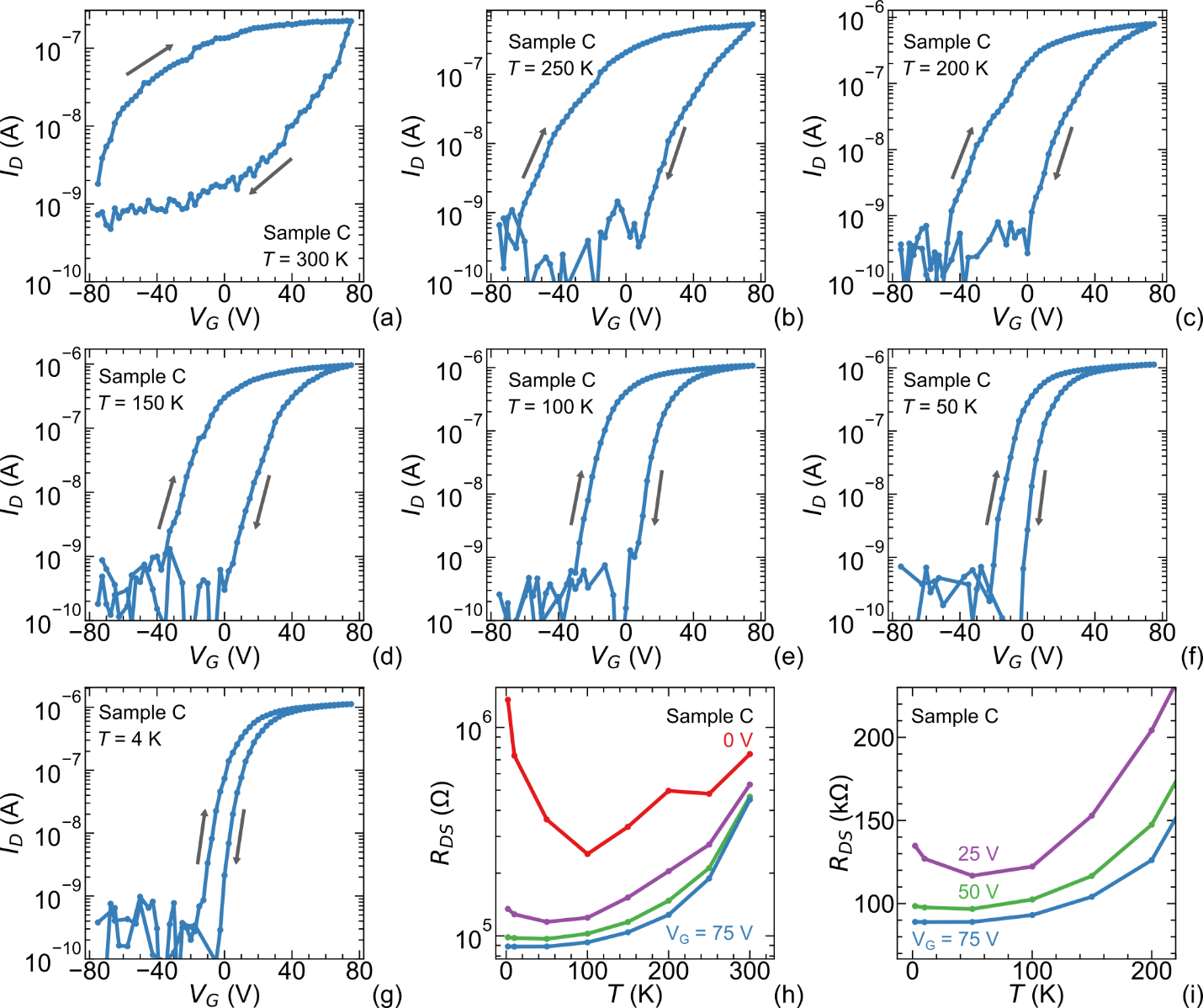
**Fig. S3.** *I*D *vs*. *V*DS data obtained in Sample A (shown in Fig. 2 of the main text in a semilog plot) plotted in the linear scale. Gate voltages *VG* was in an increasing order, *V*G = ‑75, ‑50, ‑25, 0, 25, 50, 75 V at a positive (a) and negative (b) values of *V*DS. Corresponding *I*D-*V*DS curves for decreasing *V*G at the same gate voltages are shown in (c) and (d). All measurements were done at 300 K.



**Fig. S4.** *I*D *vs*. *V*DS measured in Sample C with increasing and decreasing gate voltage measured at *T* = 300 K. The sign of the *I*D reversed for negative *V*DS to facilitate the semi-log plotting. Gate voltage *V*G was increased in (a) and decreased in (b) in 25 V increments from ‑75 V to 75 V. After *V*G was set, the *V*DS was increased then decreased from 0 to -10V and back (not shown for clarity), then from 0 V, to 10 V, to -10 V and finally to 0 V. Note that the maximum current is smaller than shown in Fig. S6 below as the data was taken after the sample was left at room temperature for an extended time, resulting in a small degradation of the sample from previous measurements.



**Fig. S5.** a-g) The transfer curves of *I*D *vs*. *V*G of Sample B, performed using the same procedure as Sample A (shown in Fig. 3 in the main text). *V*DS = 0.1 V for all measurements. VG = 25 V, 50 V, and 75 V for upper portion of loop is used for Fig. 4b in the main text.

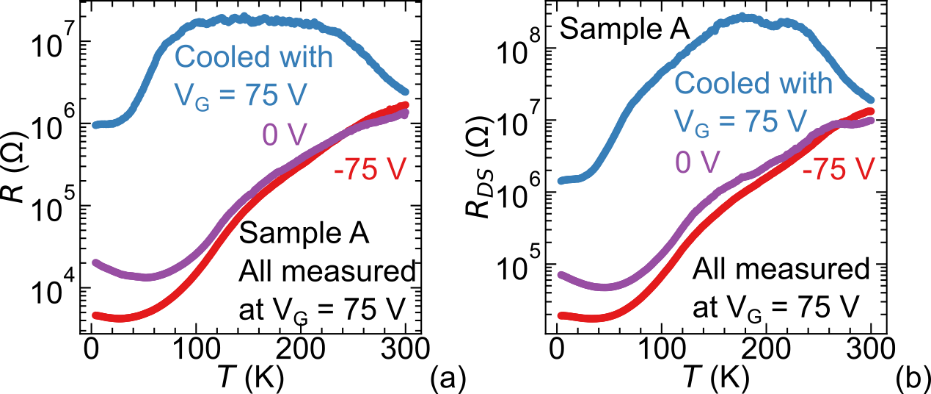


**Fig. S6.** a-g) The transfer curves of *I*D *vs*. *V*G of Sample C performed using the same procedure as Sample A shown in Fig. 3 in the main text; *V*DS = 0.1 V for all measurements. h). *R*DS(*T, VG*) taken from the clockwise hysteresis loops of *I*D *vs*. *V*G curves a-g, showing the same behavior seen in Figs. 4a-b in the main text. i) Low-temperature data from (h) shown in a linear plot for comparison.

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**Fig. S7.** a)Contact resistance between *α*-In2Se3 and Ti/Au leads measured with a *V*DS = 0.1 V bias between source and drain leads using a 3-point lead configuration at room temperature. b) 4-point resistance of the sample.

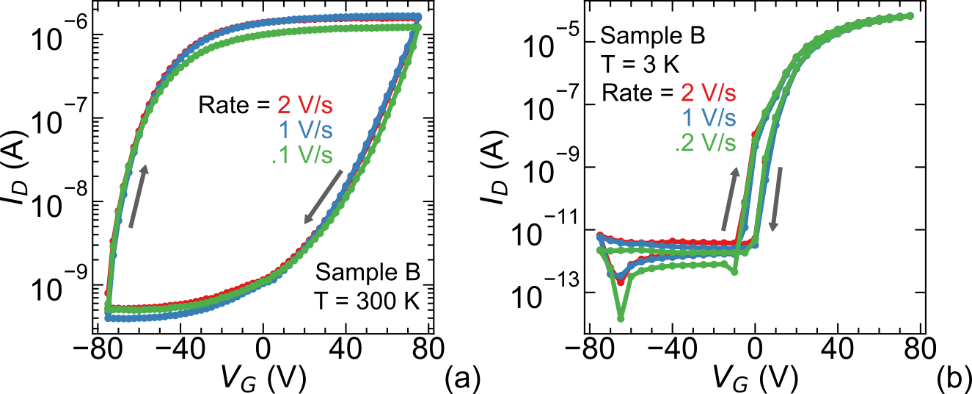
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**Fig. S8**. History dependence of *R*(T) and *R*DS(T) of Sample A. *V*G was ramped from 0 to – 75 V at 300 K, then cooled to 4K with *V*G ramped to and fixed at ‑75 V, 0 V, or 75V. At *T* = 4 K, *V*G was ramped again going through the full hysteresis loop clockwise to *V*G = 75 V before *R* was measured as a function of increasing *T* while *V*G is fixed at that value. *R* is seen to the smallest when the sample was cooled at *V*G = -75 V.

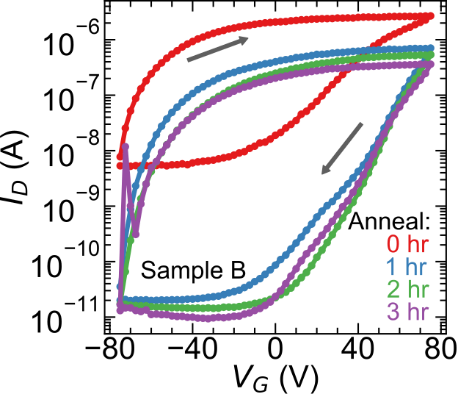
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**Fig. S9.** Detection of charge traps at the interface between *α*-In2Se3 and SiO2. a) *I*D-*V*DS, curves for Sample A before and after the “drying” - The sample was “dried” by heating to 400 K in high vacuum for one hour within the PPMS was kept at 400 K for an hour to remove water molecules trapped at the interface. b) The transfer curves of source-drain current *vs*. gate voltage, *I*D *vs*. *V*G, at 300 K before and after the “drying”. The measurements were taken immediately before and after “drying”.



**Fig. S10.** Rate dependence on hysteresis loops of Sample B. Transfer curves of *I*D *vs*. *V*G take at different sweeping rates at 300 K (a) and 3 K (b).

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**Fig. S11.** Transfer curves of source-drain current *vs*. gate voltage, *I*D *vs*. *V*G, at 300 K before and after the sample was dried by heating to 400 K in a high vacuum for one hour in the PPMS then cooled down to room temperature to be remeasured. This was repeated two additional times for a total of 3 hours of heating at 400 K.

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